DATA SHEET

74ABT16823A

18-bit bus interface D-type flip-flop with reset and enable (3-State)

Product data

2004 Feb 02

Replaces data sheet 74ABT16823A/ABTH16823A of 1998 Feb 27

Philips Semiconductors

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18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ABT16823A

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +64 mA/–32 mA
- Latch-up protection exceeds 500 mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT16823A 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ABT16823A has two 9-bit wide buffered registers with Clock Enable ($n\overline{CE}$) and Master Reset ($n\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition is transferred to the corresponding flip-flop's Q output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C; GND = 0 V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	C_L = 50 pF; V_{CC} = 5 V	2.3 1.9	ns
C_{IN}	Input capacitance	V_I = 0 V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_O = 0 V or V_{CC}; 3-State	6	pF
I_{CCZ}	Quiescent supply current	Outputs disabled; V_{CC} = 5.5 V	500	µA
I_{CCL}		Outputs low; V_{CC} = 5.5 V	9	mA

ORDERING INFORMATION

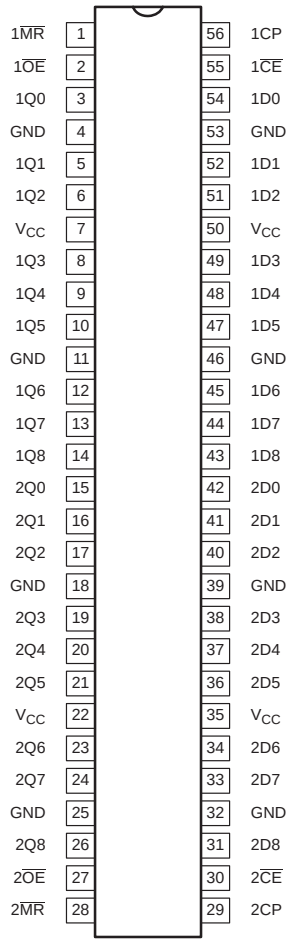
T_{amb} = –40 °C to +85 °C

Type number	Package		
	Name	Description	Version
74ABT16823ADL	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1
74ABT16823ADGG	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

PIN DESCRIPTION

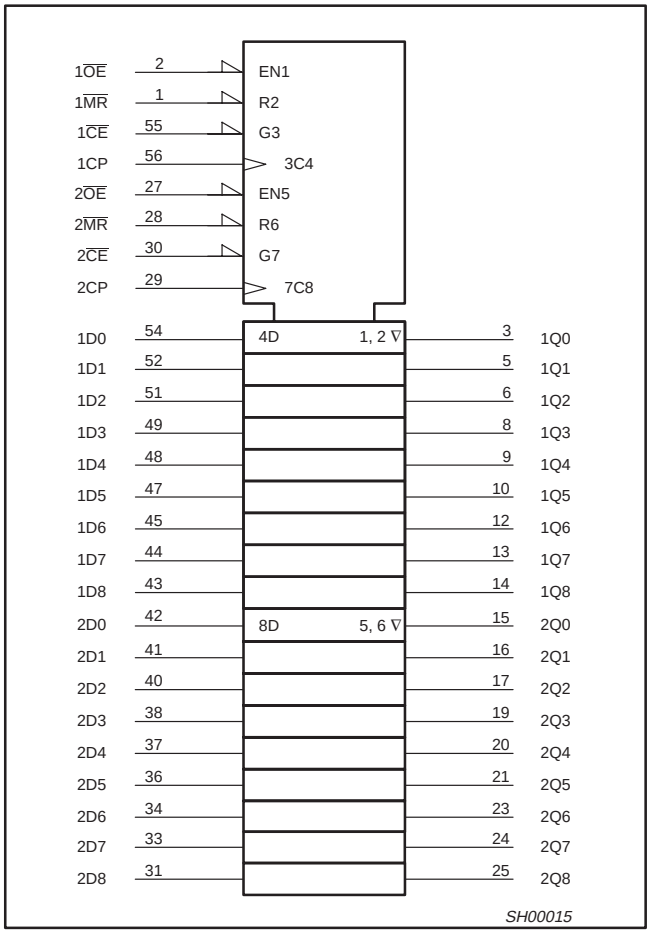
PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-LOW)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-LOW)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-LOW)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0 V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION



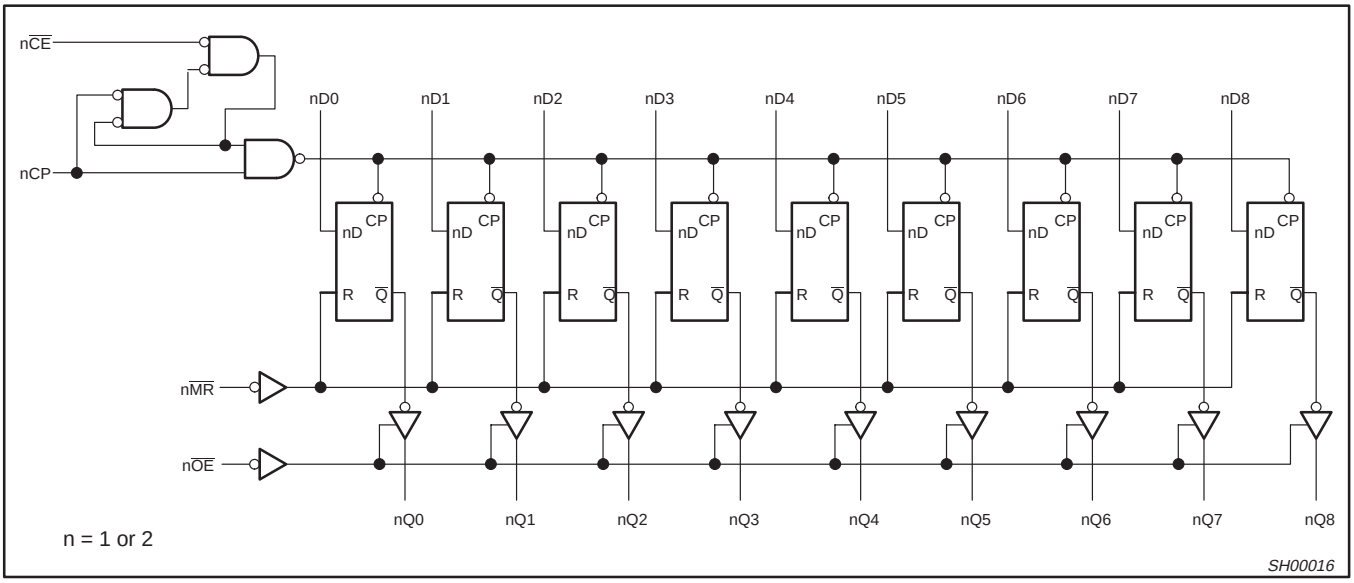
SH00014

LOGIC SYMBOL (IEEE/IEC)



SH00015

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↥	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the LOW-to-HIGH clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH clock transition
↥ = Not a LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$ V	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or HIGH state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in LOW state	128	mA
		output in HIGH state	–64	
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	HIGH-level input voltage	2.0	–	V
V_{IL}	LOW-level input voltage	–	0.8	V
I_{OH}	HIGH-level output current	–	–32	mA
I_{OL}	LOW-level output current	–	64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25 °C			T_{amb} = –40 °C to +85 °C		
			MIN	TYP	MAX	MIN	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA	–	–0.9	–1.2	–	–1.2	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	2.5	2.9	–	2.5	–	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA; V_I = V_{IL} or V_{IH}	3.0	3.4	–	3.0	–	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA; V_I = V_{IL} or V_{IH}	2.0	2.4	–	2.0	–	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}	–	0.42	0.55	–	0.55	V
V_{RST}	Power-up output LOW voltage[3]	V_{CC} = 5.5 V; I_{OL} = 1 mA; V_I = GND or V_{CC}	–	0.13	0.55	–	0.55	V
I_I	Input leakage curent	V_{CC} = 5.5 V; V_I = V_{CC} or GND	–	±0.01	±1	–	±1	µA
I_{OFF}	Power-off leakage current	V_{CC} = 0.0 V; V_O or $V_I \leq$ 4.5 V	–	±5.0	±100	–	±100	µA
$I_{PU/PD}$	Power-up/down 3-State output current[4]	V_{CC} = 2.1 V; V_O = 0.5 V; V_I = GND or V_{CC}; V_{OE} = Don't care	–	±5.0	±50	–	±50	µA
I_{OZH}	3-State output HIGH current	V_{CC} = 5.5 V; V_O = 2.7 V; V_I = V_{IL} or V_{IH}	–	1.0	10	–	10	µA
I_{OZL}	3-State output LOW current	V_{CC} = 5.5 V; V_O = 0.5 V; V_I = V_{IL} or V_{IH}	–	–1.0	–10	–	–10	µA
I_{CEX}	Output HIGH leakage current	V_{CC} = 5.5 V; V_O = 5.5 V; V_I = GND or V_{CC}	–	50	50	–	50	µA
I_O	Output current[1]	V_{CC} = 5.5 V; V_O = 2.5 V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5 V; Outputs HIGH; V_I = GND or V_{CC}	–	0.5	1	–	1	mA
I_{CCL}		V_{CC} = 5.5V; Outputs LOW; V_I = GND or V_{CC}	–	9.0	19	–	19	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3–State; V_I = GND or V_{CC}	–	0.5	1	–	1	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; one input at 3.4 V, other inputs at V_{CC} or GND	–	0.2	1	–	1	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. From V_{CC} = 2.1V to V_{CC} = 5V ± 10% a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25 °C, V_{CC} = + 5.0 V			T_{amb} = –40 °C to +85 °C, V_{CC} = +5.0 V ± 0.5 V		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	1	140	190	–	140		MHz
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	1	1.4 1.2	2.3 1.9	3.2 2.6	1.4 1.2	3.7 2.9	ns
t_{PHL}	Propagation delay n$\overline{MR}$ to nQx	2	2.0	3.3	4.3	2.0	5.0	ns
t_{PZH} t_{PZL}	Output enable time to HIGH and LOW level	4 5	1.3 1.2	2.4 2.1	3.2 2.9	1.3 1.2	3.9 3.4	ns
t_{PHZ} t_{PLZ}	Output disable time from HIGH and LOW level	4 5	1.7 1.6	2.9 2.3	4.0 3.2	1.7 1.6	4.7 3.4	ns

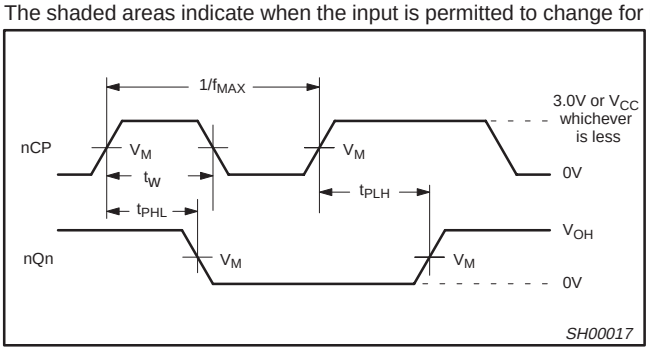
AC SET-UP REQUIREMENTS

GND = 0 V, $t_R = t_F$ = 2.5 ns, C_L = 50 pF, R_L = 500 Ω

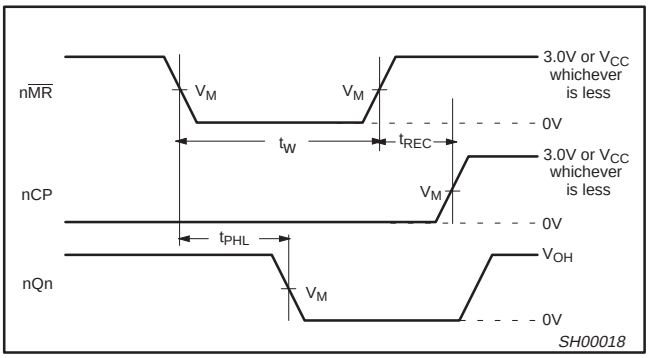
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T_{amb} = +25 °C, V_{CC} = + 5.0 V		T_{amb} = –40 °C to +85 °C, V_{CC} = +5.0 V ± 0.5V	
			MIN	TYP	MIN	
t_s(H) t_s(L)	Set-up time, HIGH or LOW nDx to nCP	3	2.0 1.5	1.3 0.9	2.0 1.5	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW nDx to nCP	3	1.5 1.5	–0.9 –1.2	1.5 1.5	ns
t_w(H) t_w(L)	nCP pulse width HIGH or LOW	1	3.3 3.3	1.7 1.7	3.3 3.3	ns
t_s(H) t_s(L)	Set-up time, HIGH or LOW n$\overline{CE}$ to nCP	3	1.5 2.0	0.9 0.9	1.5 2.0	ns
t_h(H) t_h(L)	Hold time, HIGH or LOW n$\overline{CE}$ to nCP	3	1.5 1.5	–0.8 –0.9	1.5 1.5	ns
t_w(L)	n$\overline{MR}$ pulse width, LOW	2	3.0	1.7	3.0	ns
t_{rec}	Recovery time n$\overline{MR}$ to nCP	2	2.5	1.0	2.5	ns

AC WAVEFORMS

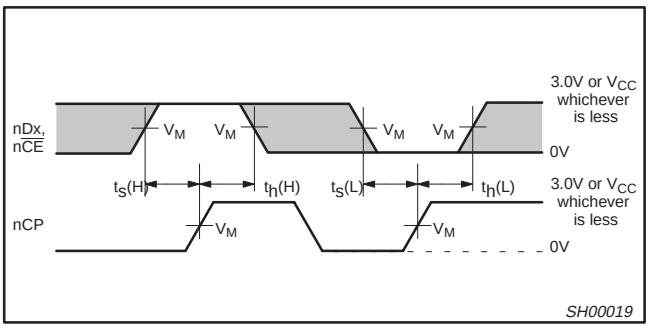
For all waveforms, V_M = 1.5 V.
The shaded areas indicate when the input is permitted to change for predictable output performance.



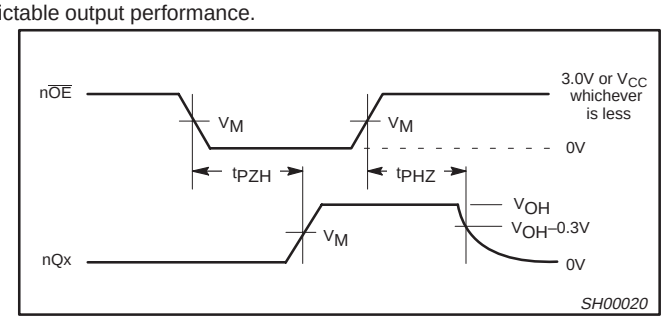
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



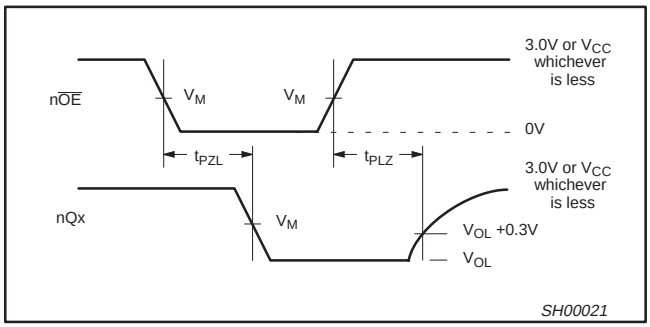
Waveform 2. Master Reset Pulse WIdth, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 3. Data Set-up and Hold Times

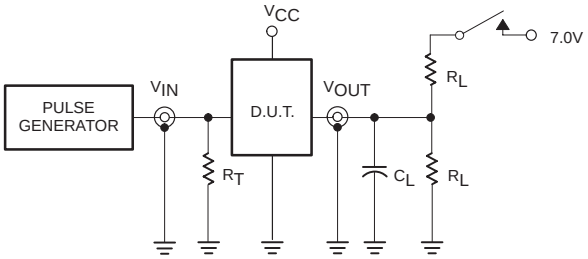


Waveform 4. 3-State Output Enable Time to HIGH Level and Output Disable Time from HIGH Level

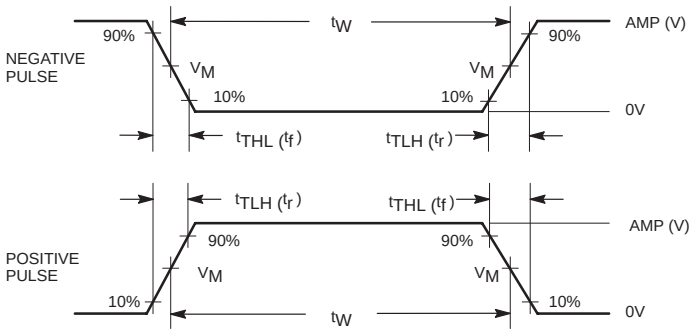


Waveform 5. 3-State Output Enable Time to LOW Level and Output Disable Time from LOW Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

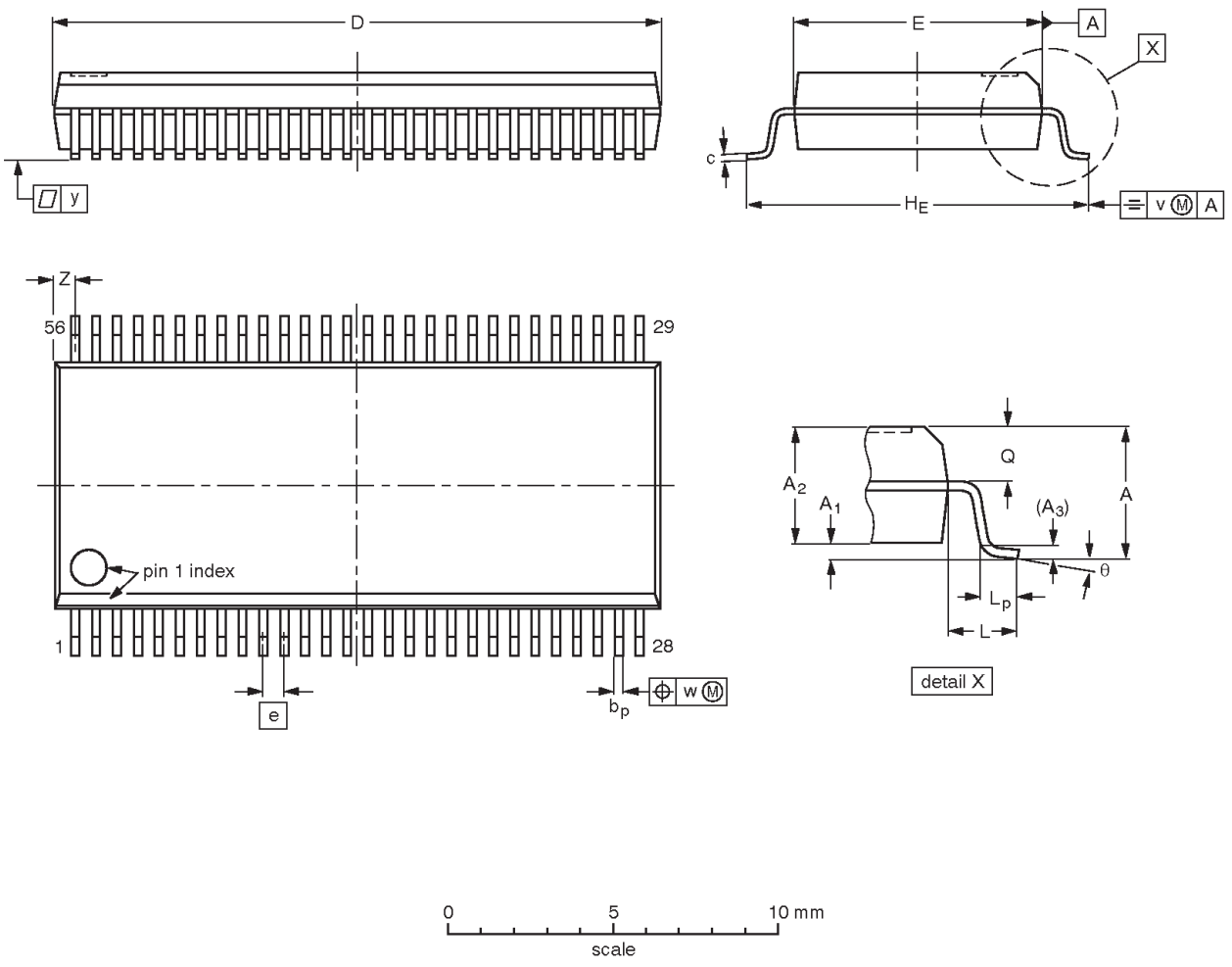
DEFINITIONS:

R_L = Load resistor; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74ABT16	3.0V	1MHz	500ns	2.5ns	2.5ns

SH00022

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

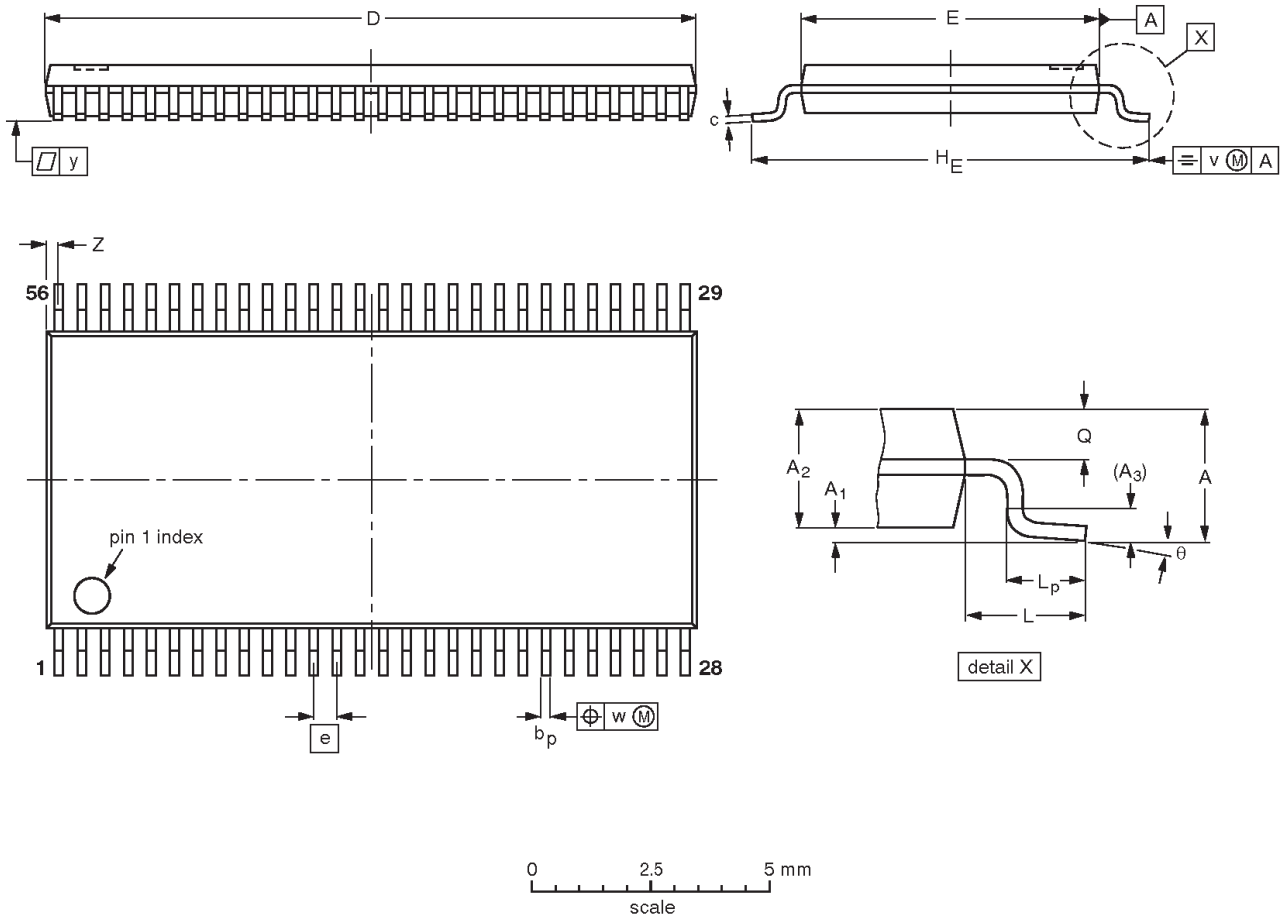
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT371-1		MO-118				~~99-12-27~~ 03-02-18

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ABT16823A

REVISION HISTORY

Rev	Date	Description
_3	20040202	**Product data (9397 750 12833); 853-1791 ECN 01-A15432 of 27 January 2004. Replaces data sheet 74ABT_H16823A_2 of 1998 February 27 (9397 750 03502).** Modifications: • Delete all references to 74ABTH16823A (product discontinued).
_2	19980227	**Product specification (9397 750 03502); ECN 853-1791 19025 of 27 February 1998. Supersedes data of 1995 Sep 28.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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